REMARKS

Claims 1-22 are all the claims pending in the application. Claim 22 is added herein. Claims 6-7, 13-14, and 20-21 stand objected to. Claims 1, 5-6, 8, 12-13, 15, and 19-20 stand rejected on prior art grounds. Applicants gratefully acknowledge that claims 2-4, 7, 9-11, 14, 16-18, and 21 would be allowable if rewritten in independent form. Applicants respectfully traverse the objections/rejections based on the following discussion.

I. The Objections to the Claims

Claims 6-7, 13-14, and 20-21 stand objected to because of informalities. Accordingly, Applicants have amended claims 6-7, 13-14, and 20-21 in accordance with the Examiner's suggestions to properly overcome the objections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections.

II. The Prior Art Rejections

Claims 1, 5-6, 8, 12-13, 15, and 19-20 stand rejected under 35 U.S.C. §102(a) as being unpatentable over Zolotov, et al. (U.S. Publication No. 2004/0044510 A1), hereinafter referred to as "Zolotov". Applicants respectfully traverse these rejections based on the following discussion.

Zolotov teaches methods for an improved fast simulator, and more particularly, methods to improve the simulation of SOI circuits. Central to Zolotov is a fast simulator which uses a fast model for each unique device as defined by device type, device width, and device number of fingers within the circuit. At the start of simulation, the circuit is audited to collect information

on each device within the netlist and the fast model database is checked to ensure that fast models for each unique device exist. If fast models are missing, a complex model for the device in question, defined within the specification as the HSPICE (or similar model) is used to generate the fast model for the device. The complex model is provided to the simulator and is an equation-based model where width, length, and number of fingers are a subset of parameters input to the model. The device is simulated with the complex model and the length, width, and number of fingers needed to create the fast model over a number of voltages to create the fast model which may be table or equation based. In the context of Zolotov, this process is called "characterization". Once fast models exist for all devices the netlist is simulated in the fast simulator using only the fast models. Zolotov further teaches methods of separating the netlist into multiple partitions which can be simulated in a distributed manner at different simulation step sizes and methods of reducing the complexity of the fast models used.

In contrast, the Applicants' invention teaches a method for circuit optimization, where optimization is defined as maximizing the use of device sizes (types, lengths, widths, and number of fingers) of which the best modeling data is available. There are two models within the context of the Applicants' invention: an interpolated model, equivalent to the complex model provided as input to Zolotov and a "characterized" or "direct fit" model which differs substantially from the definition of the fast model of Zolotov.

Within the Applicants' invention, the characterized or direct fit model may be defined as a model fit to the measurements made on hardware for a singular device type / length / width / number of fingers and the complex model defined as a model made from measurements on a multiplicity of devices with different lengths (L) / widths (W) / numbers of fingers (F) and

generated such that L, W and F become input parameters to the model. Therefore, the characterized or direct-fit model of the Applicants' invention is a product of hardware measurement for a single device (L, W, F) whereas the fast model of Zolotov is a derivative of the complex model and therefore inherently lacks the accuracy of the direct fit model of the Applicants' invention (L, W, and F were made parameters in the generation of the complex model with some accuracy lost).

In addition to model differences outlined above, additional substantial and patentable differences exist which separate the Applicants' claimed invention from the teaching of Zolotov:

1. Zolotov does not teach the concept of a parallel set of models used to simulate the circuit. Within Zolotov, the fast model is used for all netlist simulation, therefore, Zolotov, can not teach or infer back-annotation of which model is being used for each device within the netlist, nor can it teach selective replacement of devices defined by a L/W/F which does not match a direct fit model (i.e., simulatable by the interpolated model) with a different device with has an L, W, and F matching a direct fit model, such that a more accurate direct-fit model can used in simulating the circuit.

2. Zolotov does not teach or infer sensitivity analysis on each of the devices to be shifted to determine sensitivity to the shift, nor does it teach or infer presentation of the sensitivity analysis to the user for selection of the final netlist content.

3. Zolotov is simulator specific, that is, it teaches the mechanics of a fast simulator, whereas the Applicants' invention is simulator independent. The type of simulator used in the Applicants' invention is not critical or central to the concept. One concept of the Applicants invention is that models for a device be provided with a first set specific to Ls, Ws, and Fs in

measured hardware, and a second set where Ls, Ws, and Fs have been made parameters to allow simulation of devices not characterized in hardware. Also, another significant concept of the Applicants' invention is the idea of auditing the output of a simulator to determine the state of devices, identifying devices requiring the second set of models for simulation and determining their sensitivity to shifts in L, W, or F. The Applicants' invention also provides for selectively changing the L, W, and F of identified devices to match models in the first set, re-simulating, and presenting the results to the designer for final netlist selection.

With respect to claims 1, 8, and 15, the Applicants' claimed invention provides "[a] method of analyzing circuits comprising creating a set of interpolated models for transistors (devices)...." Conversely, Zolotov does not create a set of interpolated models as defined in the Applicants' claimed invention (see paragraphs [0004] and [0017] of the Applicants' specification as originally filed for a description of the meaning of interpolated model). Instead, Zolotov creates fast transistor models from a more complex model provided as input to the fast simulator (see paragraph [0039] of Zolotov).

Next, the Applicants' claimed invention provides "...creating a set of characterized (direct fit) models for said transistors (devices)...." Conversely, Zolotov creates fast models for each transistor to be simulated through a process also termed characterization described in paragraph [0039] in which any transistor to be simulated which does not have a fast simulation model the required model is built before circuit simulation. Build utilizes the accurate SPICE model (the complex model or the interpolated model of the Applicants' invention) to simulate the transistor at many different voltages to create the simplified model. This is a common technique for fast simulators, and different than the "characterized model" of the Applicants'

claimed invention which is a model not based on simplification of the complex (interpolated model) for the transistor, but is based on hardware characterization of the device; i.e., measurement of electrical parameters of a manufactured transistor (see Applicants' specification, paragraph [0022]). In Zolotov, any device defined by width, length, and fingers can be can be characterized and a simplified model is generated using the SPICE model. In the Applicants' invention, only devices (W, L, F) built in hardware and measured can have characterized models. In the Applicants' invention, Interpolated models are generated based on characterized model data and generalized to simulate devices (W, L, F) not built in hardware and measured.

Next, the Applicants' claimed invention provides, "...analyzing said transistors (devices) within a netlist for matches in said set of characterized (direct fit) models...." Conversely, Zolotov analyzes the netlist to ensure that all devices in the circuit have fast models (W, L, F). Those devices without fast models are "characterized" to generate fast models. The Applicants' invention teaches that the netlist to be simulated is audited to determine which devices have W, L, F matches to the characterized model set; i.e., the definition of "analyzing" is patentably different between Zolotov and the Applicants' claimed invention.

Next, the Applicants' claimed invention provides, "...providing a choice of using the matched characterized (direct fit) models or one of said interpolated models in designing said circuits." Conversely, Zolotov provides no choice. Devices lacking fast models have fast models generated for them prior to netlist simulation (see paragraph [0039] of Zolotov). The availability of a fast model (Zolotov teaches both analytical and table types) are a requirement of the fast simulator. The Applicants' invention has no characterized model requirement, whereby each device in the netlist may independently be simulated with either the interpolated or

characterized models.

With respect to claims 5, 12, and 19, the Applicants' claimed invention provides, "...wherein said interpolated models and said characterized (direct fit) models comprise parallel sets of models to characterize transistor sized and parameters including electrical and environmental conditions." Conversely, the complex and fast models sets of Zolotov are not used in the simulation of the netlist (see paragraphs [0039] and [0054] of Zolotov). Furthermore, the fast or characterized model of Zolotov is not equivalent to the characterized model of the Applicants' claimed invention.

With respect to claims 6, 13, and 20, the Applicants' claimed invention provides, "...recognizing transistors (devices) in said netlist which may be simulated with said characterized (direct fit) models; providing feedback information relating to which transistors (devices) use said characterized (direct fit) models; analyzing said netlist to determine which transistors (devices) using interpolated models would benefit from using said characterized (direct fit) models; simulating changes to said netlist to facilitate switching to characterized (direct fit) models; and back annotating a series of scenarios to a circuit design layout framework for designer selection."

Conversely, Zolotov can only simulate netlists with the "characterized" or fast models. Transistors without these models have models created for them. Moreover, Zolotov does not teach feedback. This is non-obvious within the bounds of Zolotov where all devices are simulated using the fast or characterized models. Again, simulation within Zolotov only occurs using the fast or characterized model. Since there is no choice of which model to use, determination of which transistors could benefit from simulation using one model vs. another is

not taught or implied in Zolotov.

Because the Zolotov simulation is only performed with fast/characterized models, there is no simulation of a netlist, revised to substitute devices with (W, L, F) that require use of the interpolated model for those with W, L, F that could be simulated with the characterized or direct-fit model. Furthermore, Zolotov does not teach back annotation to the design framework of any type. Additionally, since only one model type is available for simulation in Zolotov, back annotation of different circuit changes which attempt to move devices from one model type to another is not taught or implied.

With respect to newly added claim 22, the Applicants have incorporated a portion of claim 2 (which the Office Action indicates includes allowable subject matter) into the language of claim 1 and have presented this in newly added claim 22. Accordingly, the Applicants respectfully request immediate allowance of claim 22.

In view of the foregoing, the Applicants respectfully submit that the features defined by independent claims 1, 8, 15, and 22 contain patentable subject matter and as such, claims 1, 8, 15, and 22 are patentable. Further, dependent claims 2-7, 9-14, and 16-21 are similarly patentable not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define. Thus, the Applicants respectfully request that these rejections be reconsidered and withdrawn. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

III. Formal Matters and Conclusion

With respect to the objections to the claims, the claims have been amended, above, to overcome these objections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-22, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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